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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Maximilian Sergio

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EXAMINER

AGGARWAL, YOGESH K

ART UNIT

PAPER NUMBER

2622

NOTIFICATION DATE

DELIVERY MODE

11/13/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 09/994,384	Applicant(s) SERGIO ET AL.	
	Examiner YOGESH K. AGGARWAL	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments with respect to claims 8-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 8-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smisko (US Patent # 4,902,886), Zhang (US Patent # 5,847,599), Nair (US Patent # 6,370,270) and in further view of Dickinson et al. (US Patent # 6,631,201).

[Claim 8]

Smisko teaches a method of reading a sensor (figure 3, photodiode 108) comprising an array of photodiodes ordered in a rows connected through a row line, using a biasing and reading circuit comprising row selectors (transistor switch 116, Q1), and a charge amplifier (85) outputting a voltage of the capacitance of a selected capacitor of the array, the method comprising:

resetting an output voltage of the charge amplifier (col. 6 lines 61-63, See the timing diagram in figure 5 at 2.5) ;

connecting nonselected row and column lines of the array to a reference voltage (col. 4 lines 50-64, figure 3 teaches that the whole of the array is connected to a reference voltage V_d and since there is no switch the array is always connected to the reference voltage V_d) while connecting one of an auxiliary capacitor (feedback capacitor 122, C_f) and the selected capacitor

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(C1) to an input (198) of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier (col. 6 line 64-col. 7 line 6, figure 5 teaches that C1 and Cf are connected to the inverting input node 198 of the amplifier when the transfer switch 116 is closed at 3.0 in order to transfer first voltage to the output node) ; and

applying a step voltage (voltage shown at 3.0 in figure 5 is a step voltage applied to transfer switch 116 and capacitor C1) on the selected capacitor (C1) that is connected to the input of the amplifier and reading the output voltage at steady-state (col. 6 line 44-col. 7 line 6, figure 5 teach that the first signal that is accumulated on the capacitor C1 is outputted and read).

Smisko teaches that the invention is practiced in broadcast cameras, CCD imagers and other image sensors but fails to disclose an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors in order to selectively read pixels.

However Zhang teaches a MOS capacitive sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of MOS capacitors (imaging array 101) ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other (See figure 1) having row and column selectors col. 2 lines 45-47 teach control circuitry that is operative to sequential read pixels 103 will inherently have row and column selectors since they are used to selectively read pixels.

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Therefore taking the combined teachings of Smisko and Zhang, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors to be used in the system of Smisko as taught in Zhang in order to have an image having higher number of pixels compared to a linear scanner in order to generate an image with a better quality.

Smisko in view of Zhang fails to teach capacitive sensors. However Nair et al. teaches a CCD (charge coupled device) sensor in a camera comprises an array of light sensitive electronic capacitors (CCD sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14).

Therefore taking the combined teachings of Smisko, Zhang and Nair, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a CCD (charge coupled device) sensor as shown in Smisko be replaced by an array of a CCD (charge coupled device) sensor that comprise an array of light sensitive electronic capacitors (CCD sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14) as taught in Nair in order to determine the optimal placement locations for sensors in a given area.

Smisko in view of Zhang and Nair fails to teach pressure sensing capacitive sensors. However Dickinson et al. teaches that an image sensor 5 (figure 11) that in one embodiment is structured as an capacitive fingerprint sensor that senses pressure and an array of individual pixels (col. 9 lines 56-61). The pixels include one photodetector 73 and one switching element 71 (col. 9 lines 62-66, figure 12). The photodiode 73 has an "inherent" self capacitance (col. 10 lines 6-16). This capacitive sensor that senses pressure as well as light (since it is a

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photodetector). Therefore taking the combined teachings of Smisko, Zhang, Nair and Dickinson, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a sensor as shown in Smisko be replaced by an array of capacitive sensors that sense pressure as well as light since it comprise an array of light sensitive capacitors in order to have a device that is used to take images by sensing light and also sense fingerprints in a small, convenient, easy to use and portable device.

[Claim 9]

Zhang teaches wherein the reading of the sensor includes a sequential scanning of the pixels of the array, obtaining a frame of as many values of pixels of the sensor (col. 2 lines 45-65).

[Claim 10]

Zhang teaches that the scanning would be repeated with a certain frame frequency (col. 2 lines 55-65)

[Claim 11]

Smisko teaches a method of reading a capacitive sensor (figure 3, photodiode 108 and capacitor 114) comprising an array of capacitors (114) connected in rows (See figure 3), the method comprising:

providing a biasing and reading circuit comprising row selectors (transistor switch 116, Q1), an amplifier (85), connected to row selectors (See figure 3), for outputting a voltage of the capacitance of a selected capacitor of the array, and an auxiliary capacitor (feedback capacitor 122, Cf) connected to the row selectors (transistor switch 116, Q1);

connecting nonselected row and column lines of the array to a reference voltage (col. 4 lines 50-64, figure 3 teaches that the whole of the array is connected to a reference voltage Vd

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and since there is no switch the array is always connected to the reference voltage V_d while connecting one of an auxiliary capacitor (feedback capacitor 122, C_f) and the selected capacitor (C_1) to an inverting input (198) of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier (col. 6 line 64-col. 7 line 6, figure 5 teaches that C_1 and C_f are connected to the inverting input node 198 of the amplifier when the transfer switch 116 is closed at 3.0 in order to transfer first voltage to the output node) ; and

applying a step voltage (voltage shown at 3.0 in figure 5 is a step voltage applied to transfer switch 116 and capacitor C_1) on the selected capacitor (C_1) that is connected to the inverting input of the amplifier and reading the output voltage at steady-state (col. 6 line 44-col. 7 line 6, figure 5 teach that the first signal that is accumulated on the capacitor C_1 is outputted and read).

Smisko teaches that the invention is practiced in broadcast cameras, CCD imagers and other image sensors but fails to disclose an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors in order to selectively read pixels.

However Zhang teaches a MOS capacitive sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of MOS capacitors (imaging array 101) ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other (See figure 1) having row and column selectors col. 2 lines 45-47 teach

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control circuitry that is operative to sequential read pixels 103 will inherently have row and column selectors since they are used to selectively read pixels.

Therefore taking the combined teachings of Smisko and Zhang, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors to be used in the system of Smisko as taught in Zhang in order to have an image having higher number of pixels compared to a linear scanner in order to generate an image with a better quality.

Smisko in view of Zhang fails to teach capacitive sensors. However Nair et al. teaches a CCD (charge coupled device) sensor in a camera comprises an array of light sensitive electronic capacitors (CCD sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14).

Therefore taking the combined teachings of Smisko, Zhang and Nair, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a CCD (charge coupled device) sensor as shown in Smisko be replaced by an array of a CCD (charge coupled device) sensor that comprise an array of light sensitive electronic capacitors (CCD sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14) as taught in Nair in order to determine the optimal placement locations for sensors in a given area.

Smisko in view of Zhang and Nair fails to teach pressure sensing capacitive sensors. However Dickinson et al. teaches that an image sensor 5 (figure 11) that in one embodiment is structured as an capacitive fingerprint sensor that senses pressure and an array of individual pixels (col. 9 lines 56-61). The pixels include one photodetector 73 and one switching element

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71 (col. 9 lines 62-66, figure 12). The photodiode 73 has an "inherent" self capacitance (col. 10 lines 6-16). This capacitive sensor that senses pressure as well as light (since it is a photodetector). Therefore taking the combined teachings of Smisko, Zhang, Nair and Dickinson, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a sensor as shown in Smisko be replaced by an array of capacitive sensors that sense pressure as well as light since it comprise an array of light sensitive capacitors in order to have a device that is used to take images by sensing light and also sense fingerprints in a small, convenient, easy to use and portable device.

[Claim 12]

Zhang teaches resetting an output voltage of the charge amplifier (col. 3 lines 54-61, figure 3);

[Claims 13 and 14]

See Examiner's notes regarding claims 9 and 10 respectively.

[Claim 15]

Smisko teaches a method of reading a capacitive sensor (figure 3, photodiode 108 and capacitor 114) comprising an array of capacitors (114) ordered in rows, the system comprising:

a biasing and reading circuit comprising an amplifier (85) for outputting a voltage representing the capacitance of a selected capacitor (C1), an auxiliary capacitor (feedback capacitor 122, Cf), configuration switches (transistor switch 116, Q1) for coupling one of the auxiliary capacitor (Cf) and the selected capacitor (C1) as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier (See figure 3).

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Smisko teaches an analog-to-digital converter (figure 3, A/D converter) for converting the output voltage to digital data; an input interface circuit (transfer switches 116) for connecting deselected row lines and column lines of the array to a reference voltage and while coupling the selected capacitor of the capacitive sensor to the biasing and reading circuit (transfer switch 116 connect the pixels to a resetting voltage when the resetting switch 199 is closed, col. 6 line 46-col. 7 line 46, figure 5); a microprocessor (100) for performing noise filtering (col. 6 lines 42-46) . It would be obvious to have a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor in order to use the values of the light falling on the sensor.

Smisko teaches that the invention is practiced in broadcast cameras, CCD imagers and other image sensors but fails to disclose an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors in order to selectively read pixels.

However Zhang teaches a MOS capacitive sensor (figure 1, pixel 103, It is noted that a MOS structure comprises silicon-dioxide deposited on a silicon substrate and a conducting layer provides one capacitance plate and the substrate is the other plate and the device is called a MOS capacitive sensor) comprising an array of MOS capacitors (imaging array 101) ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other (See figure 1) having row and column selectors col. 2 lines 45-47 teach control circuitry that is operative to sequential read pixels 103 will inherently have row and column selectors since they are used to selectively read pixels.

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Therefore taking the combined teachings of Smisko and Zhang, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an image sensor ordered in a row and columns functionally connected through a row line and through column lines substantially orthogonal to each other having row and column selectors to be used in the system of Smisko as taught in Zhang in order to have an image having higher number of pixels compared to a linear scanner in order to generate an image with a better quality.

Smisko in view of Zhang fail to teach real-time correction of data. However Official Notice is taken that real-time correction of data is well known in the art in order to have a sufficiently fast and accurate system that can correct the images as fast as they are read in. Therefore taking the combined teachings of Smisko, Zhang and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have real-time correction of data is well known in the art in order to have a sufficiently fast and accurate system that can correct the images as fast as they are read in.

Smisko in view of Zhang fails to teach capacitive sensors. However Nair et al. teaches a CCD (charge coupled device) sensor in a camera comprises an array of light sensitive electronic capacitors (CCD sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14).

Therefore taking the combined teachings of Smisko, Zhang and Nair, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a CCD (charge coupled device) sensor as shown in Smisko be replaced by an array of a CCD (charge coupled device) sensor that comprise an array of light sensitive electronic capacitors (CCD

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sensor elements) that are typically placed in a grid based pattern (col. 2 lines 11-14) as taught in Nair in order to determine the optimal placement locations for sensors in a given area.

Smisko in view of Zhang and Nair fails to teach pressure sensing capacitive sensors. However Dickinson et al. teaches that an image sensor 5 (figure 11) that in one embodiment is structured as an capacitive fingerprint sensor that senses pressure and an array of individual pixels (col. 9 lines 56-61). The pixels include one photodetector 73 and one switching element 71 (col. 9 lines 62-66, figure 12). The photodiode 73 has an "inherent" self capacitance (col. 10 lines 6-16). This capacitive sensor that senses pressure as well as light (since it is a photodetector). Therefore taking the combined teachings of Smisko, Zhang, Nair and Dickinson, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a sensor as shown in Smisko be replaced by an array of capacitive sensors that sense pressure as well as light since it comprise an array of light sensitive capacitors in order to have a device that is used to take images by sensing light and also sense fingerprints in a small, convenient, easy to use and portable device.

[Claim 16]

Smisko teaches wherein FET transfer switches (116) comprise the row and column selectors that are being controlled by the microprocessor (100) that inherently has a timing generator to read the pixels at a certain according to the timing diagram of figure 5. Smisko further teaches that the amplifier (85) and A/D converter is also controlled by the microprocessor 100 (col. 6 lines 31-52, figures 3 and 5). The timing diagram and the operation will inherently be synchronized by the microprocessor.

[Claim 17]

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Smisko teaches wherein the shift register is used to read the pixels serially which means that it generates timing signals at a certain frequency (col. 1 lines 39-45). Zhang in view of Smisko fail to teach a finite state machine controlled by the microprocessor unit for configuring the shift register. However Official notice is take that it is very well known in the art to have a finite state machine that is controlled by the microprocessor unit for configuring the shift register because finite state machines can be optimized to remove redundancies and thereby reduce the time and space required to use the finite state machines. Therefore taking the combined teachings of Zhang, Smisko and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a finite state machine that is controlled by the microprocessor unit for configuring the shift register because finite state machines can be optimized to remove redundancies and thereby reduce the time and space required to use the finite state machines.

[Claim 18]

Zhou teaches a digital shift register circuit (a selection logic circuit) controlled by the microprocessor unit 100 for producing selection signals (col. 1 lines 39-45, col. 6 lines 43-46, figures 1 and 3), and a plurality of connection modules (common node 106) for connecting the deselected rows and columns to the reference voltage (V_d), and for coupling the selected capacitor to the biasing and reading circuit based upon the selection signals (col. 1 lines 39-45).

[Claims 19-24]

These claims are a combination of claims 8, 11, 15 and 16 . Therefore these claims are rejected based upon rejected claims 8, 11, 15 and 16 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH K. AGGARWAL whose telephone number is (571)272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yogesh K Aggarwal/
Examiner, Art Unit 2622